

CLAIMS

Having thus described our invention in detail, what we claim as new and desire to secure by the Letters Patent is:

1 1. A method for forming multi-depth apertures in a substrate comprising the steps of:

2
3 (a) providing a pad stack atop a surface of a substrate having regions for forming
4 apertures therein, said pad stack including at least a top patterned masking layer;

5
6 (b) blocking at least one of said regions of said substrate with a first block mask, while
7 leaving at least one other region of said substrate unblocked;

8
9 (c) forming a plurality of first apertures having a first depth in said unblocked region of
10 said substrate using said patterned masking layer to define said plurality of first
11 apertures;

12
13 (d) removing said first block mask; and

14
15 (e) forming a plurality of second apertures having a second depth in regions of said
16 substrate that were previously blocked by said first block mask using said patterned
17 masking layer to define said second apertures, while simultaneously increasing said first
18 depth such that said first depth is deeper than said second depth.

1 2. The method of Claim 1 wherein said substrate is a semiconductor substrate, a
2 conductor, an insulator or mixtures and multilayers thereof.

1 3. The method of Claim 1 wherein said pad stack further includes a pad oxide layer and
2 a pad nitride layer, wherein said pad nitride layer is formed atop said pad oxide layer.

FOI b7E b7F b7G b7H b7I b7J b7K b7L b7M b7N b7O b7P b7Q b7R b7S b7T b7U b7V b7W b7X b7Y b7Z

1 4. The method of Claim 1 wherein said patterned masking layer is a silicate glass
2 selected from the group consisting of boron doped phosphorus silicate glass and
3 tetraethylorthosilicate.

1 5. The method of Claim 1 wherein said patterned masking layer is formed by
2 deposition, lithography and etching.

1 6. The method of Claim 1 wherein said first block mask includes a first photoresist
2 layer.

1 7. The method of Claim 1 wherein said plurality of first apertures and said plurality of
2 second apertures comprise openings, trenches, grooves, notches, holes, slits, gaps, slots,
3 clefts, vias, voids, passages or mixtures thereof.

1 8. The method of Claim 1 wherein said plurality of first apertures and said plurality of
2 second apertures are formed by etching.

1 9. The method of Claim 1 wherein said etching comprises reactive-ion etching.

1 10. The method of Claim 1 further comprising blocking additional portions of said
2 substrate with a second block mask prior to conducting step (e); conducting step (e);
3 removing said second block mask; and forming a plurality of third apertures having a
4 third depth, while simultaneously increasing the first and second depths such that the
5 first depth is greater than the second depth, which is greater than the third depth.

1 11. The method of Claim 10 further comprising the steps of repeating blocking and
2 forming a plurality of apertures in each previously blocked region such that different sets
3 of apertures are formed in said substrate, each set having different depths associated
4 therewith.

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- 2 12. A method of forming multi-depth isolation regions in a semiconductor substrate
- 3 comprising the steps of:
- 4 (a) providing a pad stack atop a surface of a semiconductor substrate having regions for
- 5 forming trench isolation regions therein, said pad stack including at least a top patterned
- 6 masking layer;
- 7
- 8 (b) blocking at least one of said regions of said semiconductor substrate with a first
- 9 block mask, while leaving at least one other region of said semiconductor substrate
- 10 unblocked;
- 11
- 12 (c) forming a plurality of first trench isolation regions having a first depth in said
- 13 unblocked region of said semiconductor substrate using said patterned masking layer to
- 14 define said plurality of first trench isolation regions;
- 15
- 16 (d) removing said first block mask; and
- 17
- 18 (e) forming a plurality of second trench isolation regions having a second depth in
- 19 regions of said semiconductor substrate that were previously blocked by said first block
- 20 mask using said patterned masking layer to define said second trench isolation regions,
- 21 while simultaneously increasing said first depth such that said first depth is deeper than
- 22 said second depth.

1 13. The method of Claim 12 wherein said semiconductor substrate is selected from the
2 group consisting of Si, Ge, SiGe, GaAs, InAs, InP, Si/SiGe and silicon-on-insulator.

1 14. The method of Claim 12 wherein said pad stack further includes a pad oxide layer
2 and a pad nitride layer, wherein said pad nitride layer is formed atop said pad oxide
3 layer.

- 1 15. The method of Claim 12 wherein said patterned masking layer is boron doped
2 phosphorus silicate glass.
- 1 16. The method of Claim 12 wherein said patterned masking layer is formed by
2 deposition, lithography and etching.
- 1 17. The method of Claim 12 wherein said plurality of first apertures and said plurality of
2 second apertures are formed by reactive-ion etching.
- 1 18. The method of Claim 12 further comprising blocking additional portions of said
2 substrate with a second block mask prior to conducting step (e); conducting step (e);
3 removing said second block mask; and forming a plurality of third trench isolation
4 regions having a third depth, while simultaneously increasing the first and second depths
5 such that the first depth is greater than the second depth, which is greater than the third
6 depth.
- 1 19. The method of Claim 18 further comprising the steps of repeating blocking and
2 forming a plurality of isolation trench regions in each previously blocked region such
3 that different sets of trench isolation regions are formed in said substrate, each set having
4 different depths associated therewith.
- 1 20. The method of Claim 12 further comprising depositing a trench isolation material in
2 each of said trench isolation regions and planarizing.